Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A sample hold circuit for sampling an input potential, holding the sampled potential and outputting the same, comprising:

a first switching element receiving said input potential on one of its electrodes, and being turned on for a first period;

a second switching element connected at one of its electrodes to the other electrode of said first switching element, and being turned on for a second period;

a first capacitor connected at one of its electrodes to the other electrode of said second switching element, and receiving on the other electrode a predetermined potential; and

a drive circuit having an input node connected to the other electrode of said second switching element and an output node connected to the other electrode of said first switching element, and providing a potential corresponding to a potential of said input node to the output node wherein a power supply voltage of said drive circuit is intermittently supplied.

2. (Original) The sample hold circuit according to claim 1, wherein

said first and second periods are the same period.

3. (Original) The sample hold circuit according to claim 1, wherein

said first period contains said second period.

4. (Withdrawn) The sample hold circuit according to claim 1, wherein

said drive circuit includes:

a first level shift circuit providing a potential achieved by shifting a level of a potential of said input node by a predetermined first voltage in a certain direction, and

a second level shift circuit providing to said output node a potential achieved by shifting a level of an output potential of said first level shift circuit by a predetermined second voltage in a direction opposite to said certain potential direction.

5. (Withdrawn) The sample hold circuit according to claim 1, wherein

said drive circuit includes:

a first current limiting element receiving a first power supply potential on one of its electrodes, and

a first transistor of a first conductivity type having a first electrode connected to the other electrode of said first current limiting element, a second electrode receiving a second power supply potential and an input electrode receiving the potential of said input node, and

said second level shift circuit includes a second transistor of a second conductivity type having a first electrode receiving a third power supply potential, a second electrode connected to said output node and an input electrode connected to the other electrode of said first current limiting element.

6. (Withdrawn) The sample hold circuit according to claim 5, wherein

said drive circuit further includes:

a third transistor of a second conductivity type having a first electrode and an input electrode both connected to the other electrode of said first current limiting element, and having a second electrode connected to the first electrode of said first transistor, and

a fourth transistor of the first conductivity type having a first electrode connected to the second electrode of said second transistor, and having a second electrode and an input electrode both connected to said output node.

7. (Withdrawn) The sample hold circuit according to claim 5, wherein

said drive circuit further includes a second current limiting element connected between said output node and a line of a fourth power supply potential.

8. (Withdrawn) The sample hold circuit according to claim 7, wherein

said first and second power supply potentials are equal to each other, and

said second and fourth power supply potentials are equal to each other.

9. (Withdrawn) The sample hold circuit according to claim 7, wherein

said first and second current limiting elements include first and second resistance elements, respectively.

10. (Withdrawn) The sample hold circuit according to claim 7, wherein

said first current limiting element includes a third transistor of the second conductivity type receiving a first constant voltage on its input electrode, and

said second current limiting element includes a fourth transistor of the first conductivity type receiving a second constant voltage on its input electrode.

11. (Withdrawn) The sample hold circuit according to claim 4, wherein

said drive circuit further includes a pulse generating circuit changing a potential of a predetermined node between said first and second level shift circuits in said certain potential direction in a pulse-like fashion in response to the change of the potential of said input node in said certain potential direction.

12. (Withdrawn) The sample hold circuit according to claim 11, wherein

said pulse generating circuit includes a second capacitor connected at one of its electrodes to said first node, and having a potential at the other electrode being changed in said certain potential direction in a pulse-like fashion in response to the change of the potential of said input node in said certain potential direction.

13. (Withdrawn) The sample hold circuit according to claim 11, wherein

said pulse generating circuit includes a third switching element receiving on one of its electrodes a first power supply potential, connected at the other electrode to said predetermined node, and being turned on in a pulse-like fashion in response to change of the potential of said input node in said certain potential direction.

14. (Withdrawn) The sample hold circuit according to claim 4, wherein

said drive circuit further includes an offset-compensating circuit canceling an offset voltage.

15. (Withdrawn) The sample hold circuit according to claim 14, wherein

the output potential of said second level shift circuit is connected to a second node instead of said output node; and

said offset-compensating circuit includes:

a second capacitor,

a first switching circuit applying the potential of said input node to one of electrodes of said second capacitor and said first level shift circuit, and connecting the other electrode of said second capacitor to said predetermined node,

a second switching circuit applying the potential of said input node to the other electrode of said second capacitor, and applying the potential of said one electrode of said second capacitor 122a to said first level shift circuit instead of the potential of said input node, and

a third switching circuit applying the potential of said second node to said output node.

16. (Currently Amended/Withdrawn) The sample hold circuit according to claim 15, wherein

said offset-compensating circuit further includes a pulse generating circuit changing the potential of said predetermined node in a potential direction opposite to said certain potential direction in a pulse-like fashion while said first switching circuit is applying said input potential to one of the electrodes of said second ~~corresponding~~ capacitor and connection is kept between the other electrode of said second capacitor and said predetermined node.

17. (Cancelled)

18. (Currently Amended) An image display device comprising the sample hold circuit according to claim 1; and a liquid crystal cell connected at one of its electrodes to an output node of said drive circuit, and receiving on the other electrode ~~a common~~ the predetermined potential.

19. (Withdrawn) An image display device comprising the sample hold circuit according to claim 1; and a liquid crystal cell connected at one of its electrodes to an input node of said drive circuit, and receiving on the other electrode a common potential.

20. (Withdrawn) An image display device comprising:

the sample hold circuit according to claim 1;

a transistor having a first electrode connected to one of the electrodes of said first switching element, an input electrode connected to the other electrode of said second switching element, and a second electrode connected to the other electrode of said first capacitor;

a current supply connected to the first electrode of said transistor to pass a gradation current through said transistor during said first and second periods of the on-state of said first and second switching elements; and

an light-emitting element connected between the first electrode of said transistor and a line of a power supply potential to emit light at brightness corresponding to the current flowing through said transistor after elapsing of said first and second periods.

21. (Withdrawn) A sample hold circuit for sampling an input potential, holding the sampled potential and outputting the same, comprising:

a first switching element receiving said input potential on one of its electrodes, and being turned on for a first period;

a second switching element connected at one of its electrodes to the other electrode of said first switching element, and being turned on for a second period;

a capacitor connected at one of its electrodes to the other electrode of said second switching element, and receiving on the other electrode a predetermined potential; and

a drive circuit having an input node connected to the other electrode of said second switching element and an output node connected to the other electrode of said first switching element, and providing a potential corresponding to a potential of said input node to the output node, wherein

said drive circuit includes:

a first current limiting element receiving a first power supply potential on one of its electrodes,

a first transistor of a first conductivity type having a first electrode and an input node connected to the other electrode of said first current limiting element,

a second transistor of a second conductivity type having a first electrode connected to the second electrode of said first transistor, a second electrode receiving a second power supply potential and an input electrode receiving an potential of said input node,

a third transistor of the first conductivity type having a first electrode receiving a third power supply potential, and an input electrode connected to the other electrode of said first current limiting element, and

a fourth transistor of the second conductivity type having a first electrode connected to the second electrode of said third transistor, and having a second electrode and an input electrode connected to said output node.